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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,307	04/02/2001	Kouichi Takagi	01190/LH	9372

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,307	TAKAGI ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment A dated July 6, 2004.

2. Claims 32-46 are presented for examination. Applicant has canceled claims 1-31.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Re Claims 32-39 and 41-46

4. Claims 32-39 and 41-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashikaga, U.S. Patent 6215513, in view of Stinson et al., U.S. Patent 6127858, hereinafter Stinson.

5. In re claim 32, Ashikaga discloses a clock generating device [fig.1, 2, 5] which changes a clock frequency [pulse width] during a predetermined time [pulse generation to pulse end] [abstract], comprising:

- A reference clock generating section [clock generating unit 7] which generates a reference clock [clock] having a fixed reference frequency [predetermined] [col.5, ll.55-63].
- A delay chain section [polyphase clock generating unit 8] which produces a plurality of delay clocks having different delayed phases [clock-#] respectively with the fixed

reference frequency [e.g., 50 Hz] from the reference clock [fig.3; col.5, l.64 – col.6, l.13; col.7, l.62 – col.8, l.14].

- A switching control section [pulse width indicating unit 16] which outputs a selection signal [pulse generation trigger signal from pulse width indicating signal n+m bits] to indicated which clock is to be selected so as to change a clock frequency during a predetermined time [counts from counting unit 10] [col.6, ll.22-59; signal from decoder determines pulse width change which is related to period and hence, frequency].
- A selecting combining section [pulse output unit 11, counting unit 10, clock selecting unit 9, delay unit 17, and other associated circuitries/units] to output composite pulses [small base pulses make long pulse] having a frequency different from the fixed reference frequency during the predetermined time in accordance with the selection signal [col.6, l.14 – col.7, l.60].

6. Ashikaga did not discuss the combining of plural delay clocks.

7. Stinson discloses a clock generating device [clock variator circuit 218] which changes a clock frequency during a predetermined time [e.g., 512, 516] [abstract; fig.5; col.7, ll.3-28], comprising:

- A selecting combining section [mux 320 or interpolator 340] to select and combine plural delay clocks [D1-Dm clock signals] so as to output composite pulses [test clock #] having a frequency different from a reference frequency [clock 216] during a predetermined time [e.g., 512, 516] in accordance with a selection signal [control lines 330] [fig.5; col.2, l.44 – col.3, l.4; col.3, l.58 – col.6, l.30; col.7, ll.3-28].

8. It would have been obvious to one of ordinary skill in the art, having the teachings of Ashikaga and Stinson before him at the time the invention was made, to modify the clock generating device taught by Ashikaga to include the selecting combining section taught by Stinson, in order to obtain the selecting combining section to select and combine plural delay clocks so as to output composite pulses having a frequency different from a fixed reference frequency during a predetermined time in accordance with a selection signal. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to vary the frequency of a clock generating device that can be used to test a myriad of electronic components [Stinson: col.1, ll.12-19, ll.46-67].

9. As to claim 33, Ashikaga discloses the switching control section [pulse width indicating unit 16] that produces the selection signal [pulse generation trigger signal] based on predetermined output clock information [pulse width indicating signal n+m bits] [col.6, ll.14-38].

10. As to claim 34, Ashikaga discloses a memory section [latch, ROM, RAM] which stores the output clock information [fig.2; col.6, ll.39-59].

11. As to claim 35, Ashikaga discloses a calculating section which calculates the output clock information [col.6, ll.39-59; inherently, a calculating section in the broadest interpretation is needed to determine a pulse width in response to the modulation data indicating light and shade of an image].

12. As to claim 36, Stinson discloses the clock generating device [clock variator circuit 218] that is structured by an integral circuit [col.2, ll.44-54].

13. As to claim 37, Ashikaga discloses the clock generating device that comprises a digital circuit [fig.2; circuit operates with digital bits and control].

14. As to claim 38, Ashikaga discloses a control section which controls the clock generating device [fig.8, controller 5; col.12, ll.5-49].

15. As to claims 39 and 46, Ashikaga discloses:

- A control counter section [controller; sequences data] which produces region information [modulation data] to indicate a region to be switched [fig.7; col.10, ll.32-59], wherein:
    - The clock frequency [pulse width] is based on region data received by the control section [fig.7; col.10, l.32 – col.11, l.16].
    - The switching control section [pulse width indicating unit 16] produces the selection signal [pulse generation trigger signal j] based on the region information [[fig.7; col.10, l.32 – col.11, l.16].

16. As to claim 41, Stinson discloses a switching control section [state machine] that selects plural delay clocks so as to disperse time intervals between clocks [fig.5; col.3, l.58 – col.4, l.31].

17. As to claim 42, Stinson discloses a switching control section [state machine] that selects plural delay clocks so as to add [stretch] an optional time [fig.5; col.3, l.58 – col.4, l.31].

18. As to claim 43, Stinson discloses a switching control section [state machine] that selects plural delay clocks so as to subtract [shrink] an optional time [fig.5; col.3, l.58 – col.4, l.31].

19. As to claim 44, Stinson discloses a switching control section [state machine] that conducts a first selection to select plural delay clocks so as to add an optional time [stretch] and a second selection to select plural delay clocks so as to alternately subtract an optional time [shrink] [fig.5; col.3, l.58 – col.4, l.31; microcode varies various phases accordingly].

20. As to claim 45, Ashikaga discloses an image forming apparatus [fig.8; image recording apparatus], comprising:

- The clock generating device [see discussion above in reference to claim 32].
- A writing device [fig.5, LED print head] to write an image based on the clock output from the selecting combining section [pulse output unit 11, counting unit 10, clock selecting unit 9, delay unit 17, and other associated circuitries/units] [col.9, ll.10-60; col.10, ll.7-26; col.11, ll.17-43].
- Wherein the writing device writes an image to be located outside of a predetermined region based on the reference clock and an image to be located in the predetermined region based on the clock having a frequency different from the reference clock [col.11, ll.17-43; multi-tones have different regions].

Re Claim 40

21. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ashikaga and Stinson as applied to claim 32 above, and further in view of Guo, U.S. Patent 5451894.

22. In re claim 40, Ashikaga and Stinson disclose each and every limitation of the claim as discussed above in reference to claim 32. Ashikaga and Stinson did not discuss the details of a synchronous signal detecting section.

23. Guo discloses a clock generating device [fig.1a, 56], comprising:

- A synchronous signal detecting section [phase shift range calibrator 70] which detects the number of stages of a delay clock synchronizing with the reference clock among the plural delay clocks [fig.2, D1-Dn, 511-519; each delay stage corresponds to a different clock phase] [col.3, ll.9-45; with a constant delay for each stage, locating one particular stage in synch with the reference clock would enable the determination of the number of possible in-synch stages in a system with known finite number of delay stages].

24. It would have been obvious to one of ordinary skill in the art, having the teachings of Ashikaga, Stinson, and Guo before him at the time the invention was made, to modify the clock generating device taught by Ashikaga and Stinson to include the synchronous signal detecting section taught by Guo, in order to obtain the clock generating device comprising a synchronous signal detecting section which detects the number of stages of a delay clock synchronizing with the reference clock among the plural delay clocks. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to determine synchronization information for data recovery or other similar tasks employing a system with a plurality of delay stages [Guo: col.1, ll.47-58].

Response to Arguments

25. Applicant's arguments with respect to newly presented claim 32 have been considered but are moot in view of the new ground(s) of rejection.

26. With emphasis, as demonstrated above in reference to claim 32, the teachings of Ashikaga and Stinson to change the pulse width is analogous to changing the frequency because the basic definition of a period [T] is the inverse of frequency [f] [f = 1/T; note that frequency is denoted in Hz or 1/sec]. Thus, altering the pulse width of a signal alters the period which alters the frequency. This is in accordance with Applicant's figure 9 specifically pointed out by the Applicant in the argument.

27. Additionally, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

28. All references cited in this Office Action were cited in the previous Office Action.

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
August 20, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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